08/789,421

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/789,421	01/29/97	HARARI	E

LM41/0305

GERALD P PARSONS
MAJESTIC PARSONS SIEBERT & HSUE
FOUR EMBARCADERO CENTER
SUITE 1100
SAN FRANCISCO CA 94111-4106

EXAMINER	
HUA, L	
ART UNIT	**PAPER NUMBER**
2785	11

DATE MAILED: 03/05/98

03/05/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire Three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☑ Claim(s) 56-94 is/are pending in the application.

Of the above, claim(s) 56-62 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 63-94 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☑ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

1. The disclosure is objected to because of the following informalities: at page 5, lines 11-12, intended correction has not been made clear and not initialized at the margin by the person who made the intended correction. Appropriate correction is required.

2. Claims 63-81, 83, 84, 85, 86-90, 91, 92, and 93-94 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. As per claim 63:

i. At lines 15-16, the phrase "the addressed at least one of the memory array cell groups" lacks proper antecedent basis.

ii. At lines 20-21, the phrase "the addressed at least one of the memory array cell groups" lacks proper antecedent basis.

b. As per claim 64:

At the end of this claim, the phrase "the addressed at least one of the groups of memory array cells" lacks proper antecedent basis.

c. As per claim 65:

At the end of this claim, the phrase "the addressed at least one of the groups of memory array cells" lacks proper antecedent basis.

d. As per claims 66-81:

These claims depended on claim 63 and thus inherit the same problem of indefiniteness therefrom.

e. As per claims 83-94:

The phase "The memory" at the beginning of each of these claims lacks antecedent basis.

f. With regard to claim 83:

The phrase "any unusable ones" is not idiomatic. Grammatical error is to be corrected.

g. As per claim 84:

The phrase "the bulk storage memory" lacks antecedent basis.

h. With regard to claim 86:

The phrase "any unusable ones" is not idiomatic. Grammatical error is to be corrected.

i. With regard to claim 87:

The phrase "any unusable ones" is not idiomatic. Grammatical error is to be corrected.

j. As per claims 88-90:

These claims depended on claim 84 and thus inherit the same problem of indefiniteness therefrom.

k. As per claim 91:

The phrase "the bulk storage memory" lacks antecedent basis.

l. As per claim 92:

The phrase "the bulk storage memory" lacks antecedent basis.

m. As per claim 93:

The mapping/layout of the user-data blocks and their corresponding overhead-data units relative to the plurality of locations is not particularly and distinctly defined in the broad clause "*individual blocks of user data and corresponding units of overhead data are stored together within individual ones of a plurality of locations of the memory cell array*".

n. As per claim 94:

These claims depended on claims 83 and 84 and thus inherit the same problem of indefiniteness therefrom.

3. Claims 82, 83 and 85 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83) in view of **Tigelaar** et al (4,839,705 hereinafter referred to as **Tigelaar**) and Martinez (4,498,146).

a. As per claim 82:

i. **Burke** teaches a bulk/mass storage memory system [Fig. 1] that is:

(1) connect able to a host computer system [i.e., the host computer (claim 1)]; and

(2) comprising:

(a) an array [i.e., the semi-conductor memory (claim 1)] that is:

(i) of non-volatile memory cells [page 3, line 29, to page 4, line 2]; and

(ii) arranged to store in designated locations thereof:

1) a plurality of blocks of a given amount of user data, and

2) units of overhead data [which is inherently associated with the user data since the overhead data is information that is generally necessary for accessing the user data --- see to it that Robert S. **Lai**, "Writing MS-DOS(R) Device Drivers", second edition, teaches that his emulating semi-conductor memory is arranged to store overhead data]; and

(b) a controller [i.e., the electronic control means (claim 1)] which is:

(i) connect able [claim 1, lines 3-4] to said computer system,

(ii) for controlling operation of the array [in that it controls the array as a disk/drum controller would to a disk], and

(iii) including:

1) an addressing circuit [i.e., the means for translating (claim 1)] which is:

I responsive to receipt of a mass memory storage block address [i.e., address signals (claim 1, line 6)] from the host computer system, and

II to address, [by using the corresponding address signals (claim 1, line 8)], a corresponding block of user data and [inherently] *the unit of overhead data [which is inherently associated with the user data]*, and

2) a reading circuit, (which is inherent in order to read the user data located at the addresses indicated by his addressing circuit),

I responsive to the addressing circuit (this is to say that the reading circuit received the translated address)

II to execute an instruction from the host computer system (this is to say that the reading circuit is to either read if it receives a "read" instruction from the host computer system or to

write if it receives a "write" instruction from the host computer system).

III to perform a designated one of reading/writing user data from/to the addressed user data block.

ii. However, **Burke** does not explicitly teach:

(1) that his non-volatile memory of floating gate type, (which floating gate memory is a flash EEPROM);

(2) a reading circuit, which is responsive to his addressing circuit for reading a unit of overhead data associated with the addressed block of user data; and

(3) that his reading circuit, (which is inherent in his controller, which is for executing an instruction from his host computer system and which is to perform a designated one of reading/writing user data from/to the addressed user data block), is responsive to the read unit of overhead data.

iii. **Tigelaar** teaches a flash EEPROM, which is of floating gate type, and the principle advantage of it.

iv. **Martinez** teaches:

(1) a reading circuit, which is responsive to his addressing circuit and which is for reading a unit of overhead data associated with the addressed block of user data, in that **Martinez** teaches the combination of:

(a) means for obtaining an address for accessing a location in a storage media [col. 18, lines 56-57];

(b) means for reading contents of a table to determine if the access to the media will be impacted by defective locations;

(c) means for modifying an obtained address to compensate for the impact of defective location [col. 18, lines 61-63]; and

(2) a reading circuit, (which is inherent in **Burke**'s controller, which is for executing an instruction from **Burke**'s host computer system and which is to perform a designated one of reading/writing user data from/to the addressed user data block), and which is responsive to the read unit of overhead data, in that **Martinez** teaches a means for accessing the storage media location designated by the modified address [col 18, lines 64-67].

v. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:

(1) substitute **Burke**'s non-volatile memory with an alike memory such as that of **Tigelaar**; and

(2) add **Martinez**'s defective-location-avoiding features in the controller of **Burke**.

vi. The skilled person would have been motivated to:

(1) substitute **Burke**'s non-volatile memory with an alike memory such as that of **Tigelaar** because:

(a) **Tigelaar**'s Flash memory reduces the erasing time for erasing;

(b) **Tigelaar**'s Flash memory shrink the required array area;

(c) **Tigelaar**'s Flash memory maintains **Burke**'s non-volatility; and

(2) add **Martinez**'s defective-location-avoiding features in the controller of **Burke** because:

(a) the skilled person would have realized that **Burke**'s memory is prone to be defective and thus needs remedy;

(b) **Tigelaar**'s features provide a remedy for defective memory;

(c) **Burke** teaches error correction for providing error free data;

(d) the addition is additive in nature; and

(e) the addition provides accurate operation of a computer system in that the remedy provides error free data.

b. As per claim 83:

i. **Martinez**'s memory additionally comprises a list of any unusable ones of designated locations to link the unusable locations with others of said locations that are usable.

ii. **Martinez** teaches that his addressing circuit includes a circuit to access linked others of said locations in place of said unusable locations in that **Martinez** teaches a means for translating [col. 20, lines 8-14].

c. As per claim 85:

i. Storing a certain list as part of units of other data would have been obvious to a person having ordinary skill in the art.

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store an unusable-location list as part of overhead data associated with unusable locations.

iii. The person would have been motivated to store the units of overhead data, (associated with ususable locations), as part of the unusable-location list because:

(1) the unusable locations cannot be used to store the overhead data;

(2) the overhead data must be stored somewhere; and

(3) the locations for storing the list is usable for storing the overhead data.

4. Claims 84 and 86 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claims 82 and 83 above, and further in view of Fukushi et al. (4,757,474 hereinafter referred to as Fukushi).

a. As per claim 84:

i. **Fukushi** ('474) teaches maintaining a list of unusable locations inside a reserved locations (in PROM 5) within his memory system (Fig 3).

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that a list within a bulk storage memory system should not be maintained inside the locations which are designated to store blocks of user data and associated units of overhead data, but rather at those locations which are outside those designated locations.

iii. The skilled person would have realized this because:

(1) maintaining the list inside such designated locations would overwrite the user data and associated units of overhead data stored therein; and

(2) providing a plurality of reserved locations for storing certain information within a memory system would have been obvious to the skilled person since **Fukushi** maintains his list of unusable locations inside a reserved locations in his memory within his memory system.

b. As per claim 86:

Fukushi's unusable-location list [5] includes inoperable (or defective) locations.

5. Claim 87 is rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **common practice** in the art.

a. As per claim 87:

i. Unusable-memory-location list, including locations that contain too many defective cells such that the number of errors would be beyond the error correction capability of memory system, is **well known** in the art of memory-remapping and/or error-detection/correction.

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to the locations which have excessive number of defective cells in a list.

iii. The skilled person would have been motivated to store such locations because it is a **common practice** in the art to use both error correction and location remapping in a memory system.

6. Claim 88 is rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **SEEQ Technology, Inc.** ("512K FLASH EEPROM", October 1988, pp 2-1, 2-11).

a. As per claims 88:

i. Data blocks of the size of 512 bytes each are typical of data portions in the art of storing information into memory/storage devices. [See "48F512 512k Flash EEPROM" of **SEEQ Technology, Inc.**, for example of typical data block size].

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to arranged his memory array so that each division thereof can store a block of data having the given amount of 512 bytes.

iii. The skilled person would have been motivated to make arrangement in his memory to store 512-bytes-data block because:

(1) the nature of flash EEPROM allows an x amount of data in a block to be programmed/erased all in one sector-write operation;

(2) storing 512-bytes-data block in a sector of disk space is typical in the operation of disk storage device; and

(3) in designing a flash EEPROM device to emulate a disk storage device, the designer would likewise implement the disk device's 512-byte-per-data-block-per sector feature into the flash EEPROM device in order to not miss the 512-byte-block feature of the disk device from the flash EEPROM.

7. Claims 89 and 90 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **Wayama et al** (4,896,262 hereinafter referred to as **Wayama**).

a. As per claim 89:

Wayama teaches a semiconductor memory system that emulates a disk storage system and receives a mass-memory-storage-block address which is a magnetic-disk-sector address.

b. As per claim 90:

The inclusion of a head, cylinder and sector in a magnetic-disk-sector address is typical of a magnetic-disk-sector address. [See **Wayama** et al. (Patent Number 4,896,262), col. 5, line 25 to col. 6, line 11, for example of typical magnetic-disk-sector address which is prepared for accessing disk storage device].

8. Claims 91-93 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of Yorimoto (European Patent Application 0220718).

a. As per claim 91:

i. **Yorimoto** teaches implementing a bulk storage memory [i.e., EEPROM (12)] in a single package [i.e., IC card (10) -- Fig. 1].

ii. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a bulk storage memory in a single package as Yorimoto does to his.

iii. The skilled person would have been motivated to do this implementation because:

(1) the current advancement in semiconductor technology enables a plurality of various elements to be embedded into a single chip;

(2) the single package would be more modular and compact; and

(3) Yorimoto teach such implementation.

b. As per claim 92:

Yorimoto's bulk storage memory [12] is provided within a card [10] that is removably connect able to the computer system [i.e., external processing unit (20 -- which is called terminal device in Fig. 1)] through an electrical connector [21 -- Fig. 1].

c. As per claim 93:

Yorimoto's individual blocks of user data and corresponding units of overhead data are stored together within individual ones of a plurality of locations of the memory cell array [page 3, second col., line 21 to page 4, first col., line 30; and Figures 2, 3 and 4].

9. Claim 94 is rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar), Martinez (4,498,146) and Yorimoto (European Patent Application 0220718) as applied to claim 82 above, and further in view of **SEEQ Technology, Inc.** ("512K FLASH EEPROM", October 1988, pp 2-1, 2-11).

a. As per claim 94:

i. **Yorimoto**'s memory system inherently comprises and erasing circuit for erasing the cells within his memory locations. This is because **Yorimoto**'s data memory [12] is an electrically erasable programmable read only memory which intrinsically relies on an erasing circuit for electrically erasing its contents.

ii. However, **Yorimoto** does not explicitly teach that his inherent erasing circuit simultaneously erases the individual cells within individual locations. This because Yorimoto does not teach that his EEPROM is a flash EEPROM whose individual cells within individual locations can be simultaneously erased by an erasing circuit.

iii. **SEEQ Technology, Inc.** teaches simultaneously erasing the individual cells within individual locations [by an erasing circuit which is inherent in order to do the erasing].

iv. It would have been obvious to a skilled person having ordinary skill in the art at the time the invention was made to substitute **Yorimoto**'s EEPROM with a Flash EEPROM [such as that of SEEQ Technology, Inc.] and likewise substitute Yorimoto's inherent EEPROM-erasing circuit with an erasing circuit which is intrinsically associate with the Flash EEPROM.

v. The skilled person would have been motivated to do such substitutions because:

(1) Flash EEPROM memory is also nonvolatile similar to EEPROM memory;

(2) it is a common practice in the art to use Flash EEPROM memory to replace hard disks where the block-oriented nature is used;

(3) Flash EEPROM memory provides block-erasing capability like that of hard disks; and

(4) Flash EEPROM memory would be more efficient in term of reducing erase times.

10. Claims 63-66 and 74 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83) in view of Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146).

As per claims 63-66 and 74:

These claims do not teach above that of claims 82 rejected above.

11. Claims 67, 68, 70 and 71 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claims 82 and 83 above, and further in view of Fukushi et al. (4,757,474 hereinafter referred to as Fukushi).

As per claims 67, 68, 70 and 71:

These claims do not teach above that of claims 83 and 84 rejected above.

12. Claim 69 is rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **common practice** in the art.

As per claim 69:

This claim does not teach above that of claim 87 rejected above.

13. Claim 75 is rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **SEEQ Technology, Inc.** ("512K FLASH EEPROM", October 1988, pp 2-1, 2-11).

As per claim 75:

This claim does not teach above that of claim 88 rejected above.

14. Claims 72 and 73 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of **Wayama et al** (4,896,262 hereinafter referred to as **Wayama**).

As per claims 72 and 73

These claims do not teach above that of claims 89 and 90 rejected above.

15. Claims 76, 77 and 80 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar) and Martinez (4,498,146) as applied to claim 82 above and further in view of Yorimoto (European Patent Application 0220718).

As per claim 76:

This claim does not teach above that of claim 91 rejected above.

As per claims 77 and 80:

These claims do not teach above that of claim 92 rejected above.

16. Claims 79, 79 and 81 are rejected under 35 U.S.C. § 103 as being unpatentable over **Burk** (AU-B-22536/83), Tigelaar et al (4,839,705 hereinafter referred to as Tigelaar), Martinez (4,498,146) and Yorimoto (European Patent Application 0220718) as applied to claim 82 above, and further in view of **SEEQ Technology, Inc**. ("512K FLASH EEPROM", October 1988, pp 2-1, 2-11).

As per claim 78, 79 and 81:

These claims do not teach above that of claim 94 rejected above.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

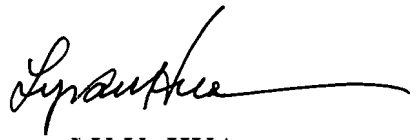
(703)305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert W. Beausoliel, Jr., can be reached on (703) 305-9713. The fax phone number for this Group is (703) 305-9742.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



LY V. HUA
PATENT EXAMINER
ART UNIT 2785

L. Hua
March 1, 1998